A timer for ultra-low-power applications and variability in sub-threshold

Authors:

Divya Akella

Patricia Gonzalez

Professor:

Mircea Stan

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1. Introduction

Sub-threshold operation scales VDD below Vthreshold, limiting performance but giving considerable energy savings [1]. Energy constrain applications has been benefited from sub-threshold operation, since this technique has opened the possibility to build Integrated Circuits able to operate at 19uW while extracting ECG and EEG features and transmitting it wireless [2]. Although, whole system integration has been proven, one of the biggest challenges that this technique faces is the high sensitivity to transistor mismatch, power supply noise and temperature [3]. This sensitivity is worsened by the scaling in technology and VDD leading to delay variability dramatically affecting the functional yield requirement [4]. In order to increase the yield we propose an architecture that adjusts VDD and frequency, so we hit the targeted delay even though we change the energy operation point.

2. Research Problem

Circuits operating at sub-threshold are very sensitive to variations. Up until now, the voltage is adjusted so the circuits work at a given frequency operation. However this approach does not have into account that variations affect the delay in such a way, that a representative percentage of dies in a wafer fail [4]. In this work we want to study variation effect in a timer and propose a methodology to improve the immunity in sub-threshold operation.

3. Circuit Proposal

3.1. Description

For this project we propose a simplified system to adjust both, VDD and Frequency so that the throughput requirement is met. Figure below shows a block diagram of the proposed architecture.

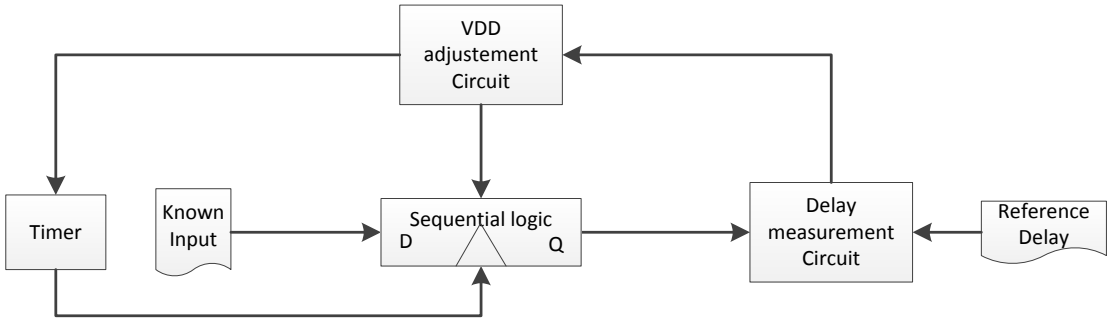

Figure 1. System Block Diagram

The timer controls the sequence of events in the sequential logic. The sequential logic receives a known pattern input that for this case might be a single bit line. The delay at the output at the sequential logic is measured to be compared with a reference delay. If the delay is longer than the reference delay then VDD is adjusted so that the frequency is increased and the delay time is corrected. The figure below shows a time diagram exemplifying the delay that should be detected by the sequential Delay measurement circuit.

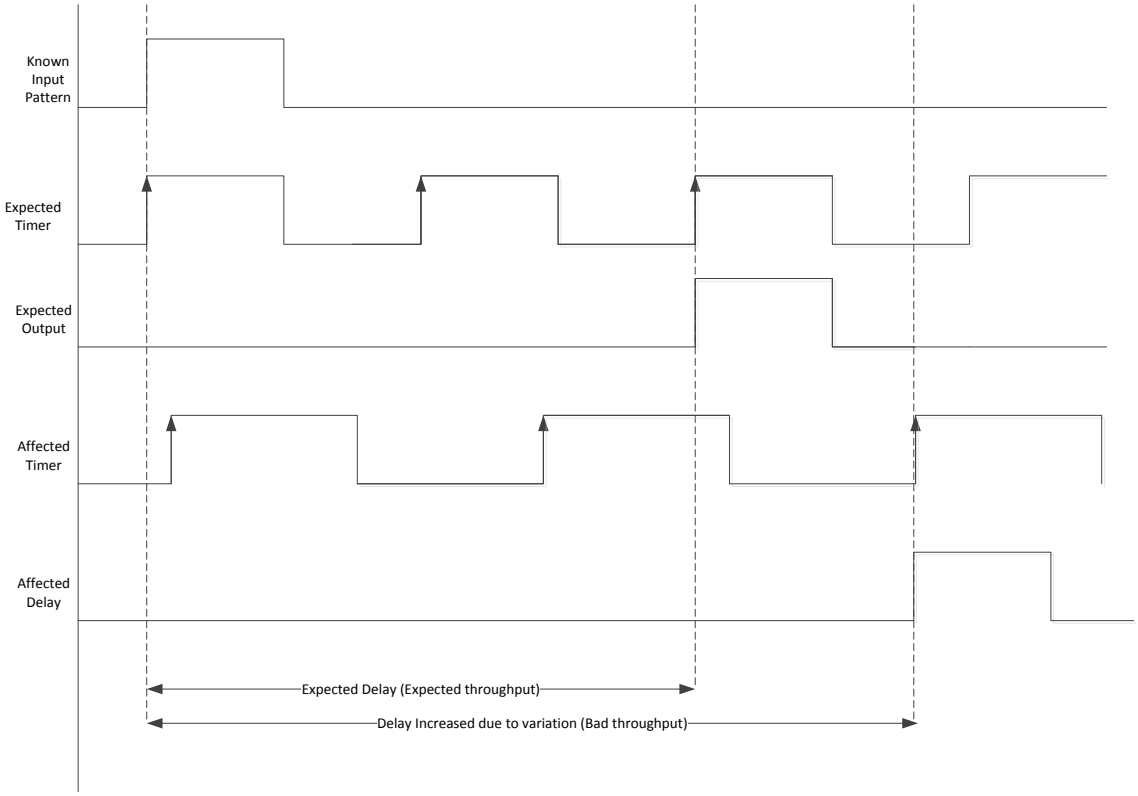

Figure 2 Timing diagram exemplifying the difference between the expected delay and the delay due to variations.

The sections below explain each component of the block diagram in detail.

3.1.1. Timer

Recently, many ultra-low power sensors, which have long idle times, have come up and are required to wake up from idle mode after certain intervals of time. Crystal oscillators, which have small sensitivity to voltage and temperature, cannot be used in these areas because of the high frequency range of operation and high power consumption. A low power timer designed using the gate leakage of MOS capacitors has been presented in [5].

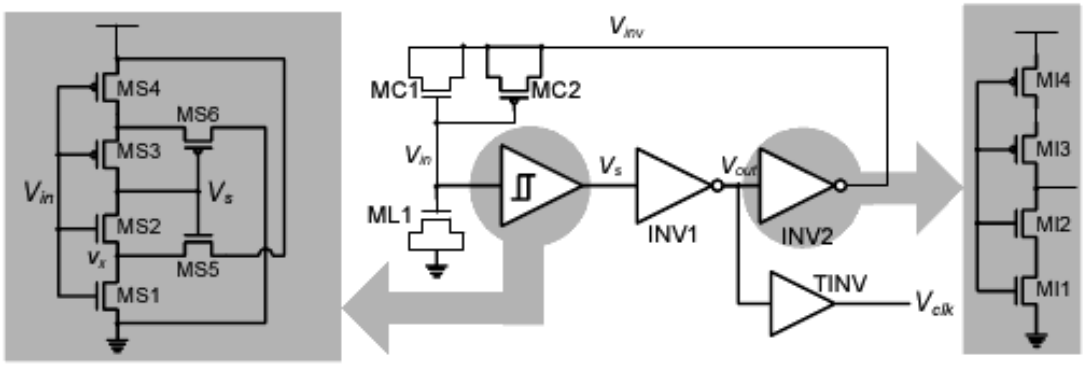

Figure 3. Low power timer circuit proposed in [1]

Variations manifest themselves while designing any integrated circuit in the global as well as local circuit performance. For the low power timer circuit from [5], the measured temperature sensitivity is 0.16%/◦ C at 600mV and is 0.6%/◦ C at 300mV; Supply sensitivity is 0.15%/mV from 300mV to 500mV and 0.04%/mV at 600mV. At 300mV, the power consumption of the timer is less than 1pW at 20◦ C and it consumes roughly 2nW at 600mV. Die-to-die variation is 28% and 27% at supply voltage of 300mV and 600mV respectively. Within-die variation is obtained by taking the average of σ/μ within individual die and is measured at 12.4% and 9.2% for 300mV and 600mV. Key sources of variation include oxide thickness variation and the voltage shift of Schmitt trigger trip points VM+ and VM− due to transistor mismatch.

3.1.2. Delay Measure Circuit

Several Built-in self-test (BIST) circuits has been proposed and implemented in practical applications in super-threshold operation, however a lot less has been studied for sub-threshold operation. In this work we will implement a delay measurement circuit to be embedded in the chip. For super-threshold operation several techniques has been proposed as fast counters[6], analog methods based on generating a voltage ramp[7] CMOs tapped delay configurations[8] and vernier delay line[9]. The analog time to voltage converter proposed in [7] seems suitable for this project due to its simplicity; however we are still studying the tradeoffs of other architectures to choose the right one for our project.

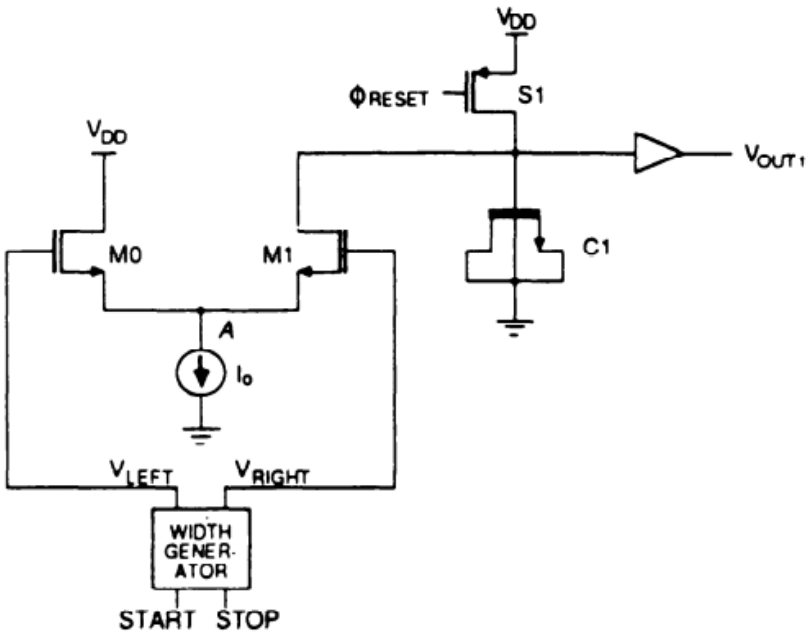

Figure 4 Single channel VTC proposed in [3]

3.1.3. Test circuit

The test circuit is intended to emulate a typical critical path delay in a sub-threshold system. This circuit can be a chain of digital gates such as inverters mixed with flip flops.

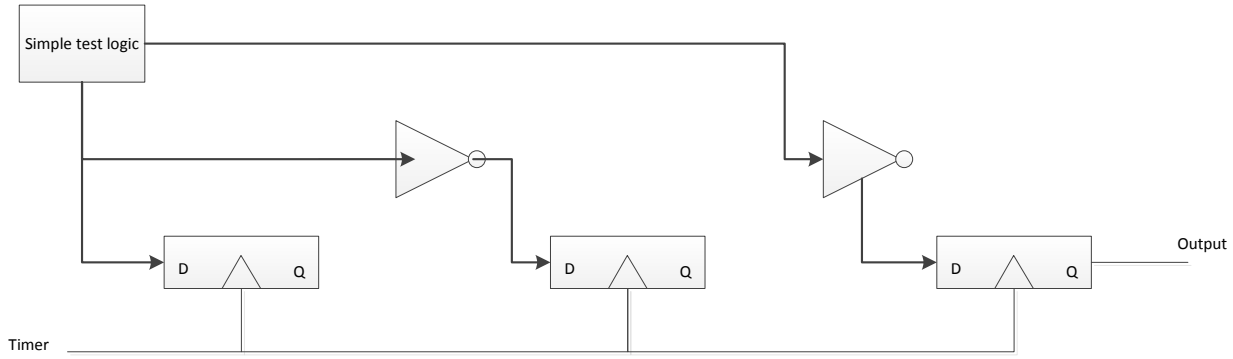

Figure 5 Simplified version of the test circuit

3.1.4. VDD adjustment circuit

DVS[10], UDVS[11] PDVS[12] are very popular in sub-threshold operation, all this solutions assume a fixed VDD and Frequency according with performance requirements. In this project we propose a variable frequency through a VDD adjustment to achieve a minimum delay required for the chip to be functional. Since our model has to be a simplified version of VDD adjustments, we propose to use different voltage references as discussed in [13]. The adjustment of which voltage reference to use will depend on the delay measurement. If the delay at the output of the test circuit is too long VDD should be increased triggering an upgrade in VDD. Figure below shows the schematics of the voltage reference proposed in [13]

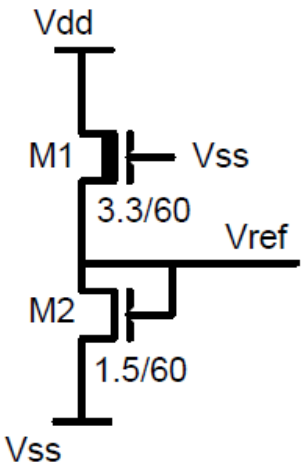

Figure 6 Voltage reference proposed in []

3.2. Main goals

With this proposed architecture we will study how variations affect the delay in a sub-threshold timer using Montecarlo simulations. After this we will implement the delay measurement circuit and its

interface with the VDD adjustment circuit. We expect to improve the percentage of functional systems under the effect of variation with our proposed architecture. Finally we will study the tradeoff between operation energy point vs. delay variation compensation, besides we will estimate the extra power consumed by the architecture proposed and compare it with the power consumption of a real sub-threshold system.

4. Chronogram

4.1. Chronogram

The table below shows the chronogram as shown in the design review to indicate progress.

Date Start	Date Finish	Milestone	Activity	Done %
		Pre-Proposal Activities	Determine areas of interest	100
			Choose the project	100
			Look for publications	80
			Discuss with Professor	80
			Define the requirements	80
			Sketch the proposal	100
	4-Oct		Preliminar simulations	100
5-Oct	12-Oct	Proposal	Write Proposal	100
13-Oct	15-Oct	Develop Project	Choose circuit topology	60
16-Oct	19-Oct		Calculations	20
20-Oct	21-Oct		Draw the schematics	20
22-Oct	27-Oct		Run simulations	5
28-Oct	30-Oct		Draw the layout	0
31-Oct	1-Nov		Run DRC	0
2-Nov	3-Nov		Run LVC	0
10-Nov	16-Nov		Run Simulations including variation	0
17-Nov	-	Evaluation	Evaluate Performance	0
-	23-Nov		Make changes	0
24-Nov	3-Dec	Final Report	Write final report	0
4-Dec	4-Dec		Present Final Report	0

4.2. Tasks division

Functional Blocks	Owner
Timer.	Divya
Sequential Logic.	Patricia
Delay Measurement circuit.	Divya
Sequential test logic.	Patricia

VDD adjustment.	Divya
Delay measurement circuit – Vdd adjustement integration.	Divya and Patricia
Delay measurement circuit – Reference delay format.	Divya and Patricia

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